

Hardware Design Guide

1. Introduction

This document provides basic design and layout guidelines to achieve the best performance for implementing a 2-layer board design.

PA1688 provide a whole low-cost solution for IP phone with single-chip ,integrated dual-processor,controller ,digital signal processor and other necessary interface including RS232,USB,SDRAM,AC97codec,SRAM and Keyboard.

PA1688 driving power is weak , so care need to be taken to make the trace as short as possible.

2.Route rule:

- ✓ PA1688 connect two latches, which latch 8-bit address bus and 24-bit data bus, trace should be as short as possible.
- ✓ PA1688 connect SDRAM by 14-bit address and 16-bit data bus, the trace also should be as short as possible.
- ✓ PA1688 connect codec ,the route also should be as short as possible ,and other circuit shouldn't in the around area, the layout and route of this area decide the quality of phone voice.
- ✓ The part of PA1688 connect programming flash ,it haven't strict requirement, but the route also should be as short as possible after it can reach the other part's requirements.
- ✓ The parts of DFAD[0]~DFAD[7] 、 KEYPAD[0]~ KEYPAD[6] and PIO[0]~PIO[16] haven't strict requirement for the route

When layouting ,latch,sdram,codec are more important than other parts ,so we should think much of these firstly.

When pcb debug, pls run coding of G723 and G729 ,it can show that if the layout of Pflash and sdram pass the requirement.

General Guidelines

- ✓ Provide a good power source , minimizing noise from other component
- ✓ Verify the quality of critical components such as clock and transformer to meet application requirements
- ✓ Keep power and ground noise levels below 100mV
- ✓ Use bulk capacitor (4.7uF-10uF) between the power and ground planes
- ✓ Use 0.1uF de-coupling capacitors as close and possible to corresponding IC such as PA1688 ,WM9707 RTL8305SB and RTL8019AS.

Differential signal layout guidelines

- ✓ Keep differential pairs as close as possible and route both traces as identically as possible.
- ✓ Avoid vias and layer changes if possible
- ✓ Keep transmit and receive pairs away from each other, run orthogonal or separate by a ground plane

Colok circuit

- ✓ Surround the clock by ground trace to minimize the high-frequency emission, if possible
- ✓ Keep the crystal or oscillator as close to corresponding IC as short as possible such as PA1688 , WM9707, RTL8305SB,RTL8019AS.
- ✓ Connect the shell of crystal with ground to enhance EMC capability.
- ✓ Don't route other trace under the crystal to deduce the interference.

Power planes

- ✓ Divide the power plane into digital and analog
- ✓ Use 0.1uF de-coupling capacitors and bulk capacitors between each power plane and grounds plane
- ✓ Power line connecting from source to the main IC pin should be at least 10 width

Ground planes

- ✓ Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board
- ✓ Place a meat (gap) between the system ground and chassis ground
- ✓ Ensure the chassis ground area is voided at some point that no ground loop exists on the chassis ground area

3.recommended IC List

- ✓ CODEC : WM9703(EOL) 、 WM9707(Wolfson)
ALC201A (REALTECH)
- ✓ SDRAM: firstly, IC42S16100 -7T(ICIS)
Secondly,M12L16161A 7T(ESMT)、 HY57V16161A(HY)
Advise not to use sdr. (Mircon)
- ✓ LATCH: HA373 (TI) 、 HA573 (TI) ,
All SDRAM whose access time less 9ns is suitable.
- ✓ RESET IC: 74HC14D (PHILIP) ,integrated Schmitt trigger
- ✓ PFLASH: MX29LV008T (MXIC)、 MX29LV800T (MXIC)
access time at least 70ns,
PA1688 can provide data bus up to 24bit,so it can support programming flash with 16M byte.
MT28F016S5
- ✓ KEYBOARD: When make a array, fault resistance of landscape array is pull up, that of horrent array is pull down.
- ✓ LCD: PA1688 haven't LCD controller, so choose LCD who integrate controller, now designed software is based on Controller of HD44780 , and it can capability with HD44780,ED1278, KS0066 and NJU6408.

4.FAQ:

- ✓ ringing voice of IP phone is weaker than common phone .
because the ringing voltage of common phone is $\pm 48V$. and that of IP phone is $\pm 5V$.

adding IC LM386 can amplify voltage to supply a high one.

- ✓ PA1688 only reads the signal of ready from LCD every cycle, it is too slow especially in matrix LCD. To solve this, LCD can be taken as a common peripheral equipment. PA1688 connects LCD by address bus, then 8051 module portmap to address 5000-5FFF to improve the performance speed. Many components can connect in this way such as RTL8019AS, MODEM.
- ✓ LCM: PA1688 hasn't integrated LCM controller, now our developed software is based on LCM with controller of HD44780 (HITACHI), and its capability with controller of SED1278 (SEIKO EPSON), KS0066 (SAMSUNG), NJU6408 (NER JAPAN RADIO).
- ✓ Speed matching of PA1688 with Programming Flash
 1. PA1688 has a turbo-8051 MCU, standard Intel 8051 needs 12 clock cycles to execute an instruction, and PA1688 only needs 4-8 clock cycles, the exact cycles depend on different instructions.
 2. As PA1688 executes an instruction at least every 4 clock cycles, it means it costs 4 clock cycles to fetch (read) an instruction from programming flash. The 8051 core can run up to 50MHz, which is 20ns per clock cycle. So ideally, $20\text{ns} \times 4 = 80\text{ns}$, a 80ns programming flash can do it. However, considering ascending and descending edges, so in practical usage, even 70ns programming flash can only run 33MHz, and 90ns programming flash can only run 22-26MHz. In present IP-phones, choose 70ns programming flash.
 3. DSP of PA1688 also can run up to 50MHz, and it runs over 40MHz in our programming flash. So in our chip, we have registers to add "wait state" for 8051 to fetch instructions and run slower. It is just because of this "wait state", our 8051 timers are no more accurate after "wait state" is added.
 4. PA1688 can run 8051 on SRAM, it is very easy and cheap to find a 20-30ns SRAM (typical TI DSPs using SRAM less than 10ns today), so 8051 and DSP of PA1688 can both run at 50MHz without wait state. Actually no SRAM can reach the speed so far.
- ✓ speed matching of Programming flash with latch

If use 70ns programming flash, at the same time run 8051 at 33MHz. It needs latch to run at very high speed. First, divide 70ns by 4 (PA1688 executes an instruction at least every 4 clock cycles, and latch works on every clock cycle), and then, as PA1688's address 8-23 shares 8 signals by latch, so speed is divided by 2 again. So matching with a 70ns programming flash, latch speed should be $70/8 = 8.75\text{ns}$. So far, we only know TI's HA373 can be so fast.